

*Preliminary Specifications Subject to Change without Notice*

#### DESCRIPTION

JW<sup>®</sup>7726B is a synchronous rectifier controller, used for the secondary side rectification of isolation topologies, such as Active Clamp Flyback and CCM/QR/DCM Flyback. By driving an external MOSFET, JW7726B is able to significantly improve the efficiency comparing with the conventional diode rectifier.

When JW7726B senses  $V_{ds}$  of MOSFET less than  $-140mV$ , it turns on the MOSFET. Once the  $V_{ds}$  is greater than  $-3mV$ , JW7726B turns off the MOSFET.

JW7726B supports multiple operation modes, such as DCM, CrCM, CCM and Quasi-Resonant. By implementing the Joulwatt proprietary technology, JW7726B is able to handle CCM operation.

JW7726B is available in SOT23-6 package.

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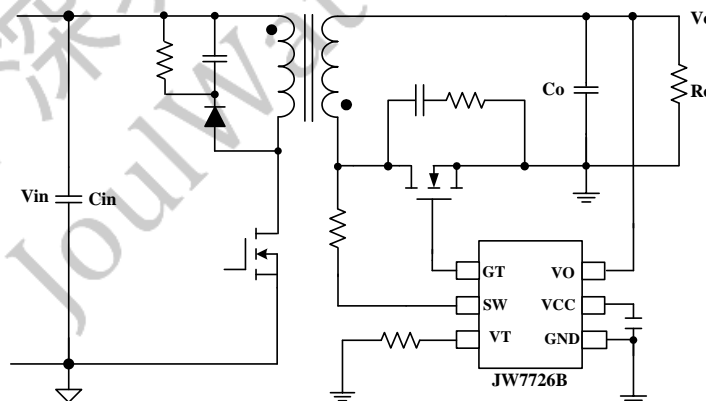
#### FEATURES

- Supports Active Clamp Flyback, DCM, Quasi-Resonant, and CCM Flyback
- Support High-side and Low-side Rectification
- Output Voltage Directly Supply VCC
- Low Quiescent Current
- Fast Driver Capability for CCM Operation
- SOT23-6 Package

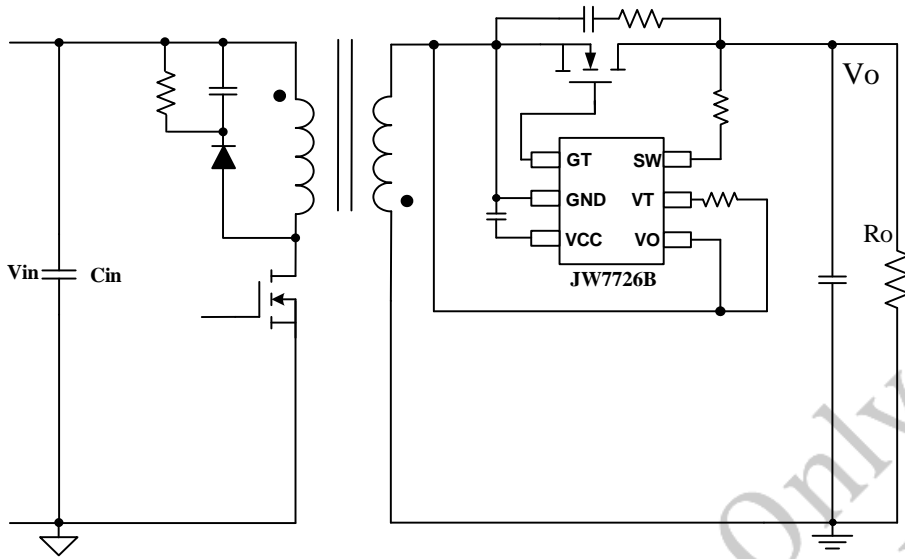
#### APPLICATIONS

- Active Clamp Flyback and Flyback Converters
- Adaptor
- LCD and PDP TV

#### TYPICAL APPLICATION



**JW7726B Typical Application for Low-side.**



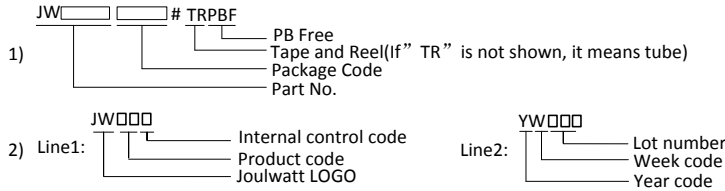
JW7726B Typical Application for High-side.

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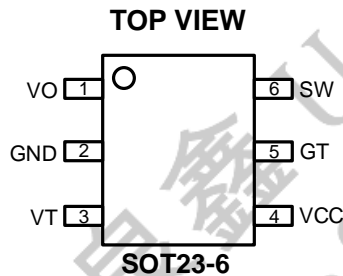
**ORDER INFORMATION**

DEVICE <sup>1)</sup>	PACKAGE	TOP MARKING <sup>2)</sup>
JW7726BSOTB#TRPBF	SOT23-6	JWEW□ YW□□□

**Notes:**



**PIN CONFIGURATION**



**ABSOLUTE MAXIMUM RATING<sup>1)</sup>**

SW PIN .....	-1 to 140V
VO PIN .....	-0.3 to 28V
VCC, GT PIN.....	-0.3 to 9V
VT PIN.....	-0.3 to 7V
Junction Temperature <sup>2) 3)</sup> .....	150°C
Lead Temperature .....	260°C
Storage Temperature.....	-65°C to 150°C
Continuous Power Dissipation(T <sub>A</sub> =+25°C) <sup>4)</sup> SOT23-6.....	0.56W
ESD Susceptibility (Human Body Model) .....	2kV

**RECOMMENDED OPERATING CONDITIONS**

SW Pin.....	4.7V to 120V
VO Pin.....	4.7V to 25V
VCC, GT PIN.....	4V to 8.5V
Operation Junction Temperature(T <sub>J</sub> ).....	-40°C to 125°C

**THERMAL PERFORMANCE<sup>5)</sup>**

	$\theta_{JA}$	$\theta_{JC}$
SOT23-6.....	220	130°C/W

**Note:**

- 1) Exceeding these ratings may damage the device. These stress rating do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$ .
- 5) Measured on JESD51-7, 4-layer PCB.

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**ELECTRICAL CHARACTERISTICS**

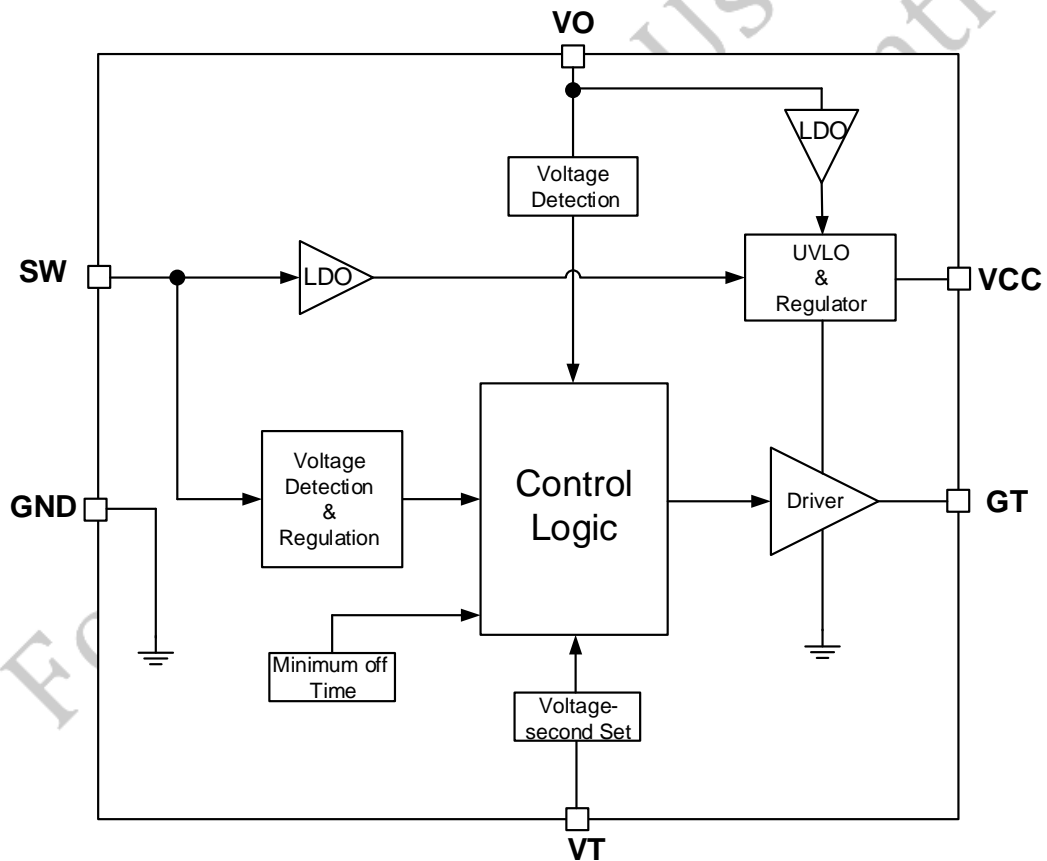
<i>TA = 25°C, unless otherwise stated</i>						
<b>Item</b>	<b>Symbol</b>	<b>Condition</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>
<i>VCC Section</i>						
VCC Voltage	VCC	SW=40V, VCC=2.2uF	7.5	8	8.5	V
VCC Startup Voltage	V <sub>CC_Startup</sub>		4.2	4.5	4.8	V
VCC UVLO	V <sub>CC_UVLO</sub>		3.8	3.95	4.1	V
Operation Current (GT On)	I <sub>VCC</sub>	GT=5nF, VCC=2.2uF	0.7	0.9	1.1	mA
Quiescent Current	I <sub>q</sub>	VCC=4.5V, VCC=2.2uF	95	110	125	uA
<i>Gate Section</i>						
Gate Turn On Threshold	V <sub>MOS_ON</sub>		-162	-140	-116	mV
Gate Turn Off Threshold	V <sub>MOS_OFF</sub>		-15	-3	10	mV
Gate Turn On Voltage	V <sub>GT</sub>	SW=32V, VCC=2.2uF	V <sub>CC</sub> -1	V <sub>CC</sub>		V
Maximum Gate Pull Up Current <sup>6)</sup>	I <sub>GU</sub>			0.6		A
Maximum Gate Pull Down Current <sup>6)</sup>	I <sub>GD</sub>			4		A
Gate Minimum On Time	T <sub>MIN_ON</sub>		520	560	600	ns
Absolutely Minimum Off Time	T <sub>MIN_OFF</sub>		280	330	380	ns
Turn-on Total Delay <sup>6)</sup>	T <sub>DON</sub>	C <sub>LOAD</sub> =4.7nF		50		ns
Turn-off Total Delay <sup>6)</sup>	T <sub>DOF</sub>	C <sub>LOAD</sub> =4.7nF		20		ns
<i>SW and VO Section</i>						
VCC Charge Current	I <sub>SW_CHG</sub>	SW=40V, VCC=6V	75	85		mA
SW Regulation Voltage	V <sub>MOS_REG</sub>		-50	-40	-20	mV
SW Control Voltage MAX	V <sub>MOS_REG_MAX</sub>		-185	-160	-145	mV
VO Enable Charge Voltage	V <sub>O_EN</sub>	VCC=4V, SW=0V, rising	4.5	4.6	4.7	V
VO Disable Charge Voltage	V <sub>O_DIS</sub>	VCC=4V, SW=0V, falling	4.4	4.5	4.6	V
VO Charge Current	I <sub>VO_CHG</sub>	SW=0V, VCC=6V, VO=12V	30	40		mA

6) Guaranteed by design.

PIN DESCRIPTION

Part No. SOT23-6	Name	Description
1	VO	Output voltage sensing and charging to VCC.
2	GND	Ground.
3	VT	Set the voltage-second product.
4	VCC	Power supply. Bypass a capacitor between VCC and GND.
5	GT	Drive the external MOSFET.
6	SW	External power MOSFET drain voltage sensing. Charging to VCC.

BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### Operation

JW7726B is a synchronous rectifier controller which combined with external MOSFET can replace the Schottky Barrier Diode. It supports all operations, such as DCM, CrCM, (Quasi-Resonant) and CCM when adopted in Active Clamp Flyback and Flyback converters.

### Startup

During the startup period, when the VCC is charged up by the two internal LDOs connected to SW and VO pin respectively.

When VO is lower than 4.5V (falling), JW7726B can power itself through the internal LDO connected to SW pin during the SR turn-off period, which means primary the primary side MOSFET is turned on and SW presents a positive voltage. A capacitor between VCC and GND is required to store the energy and supply to IC during the SR turn-on period.

When VO is above 4.6V (rising), the VO pin charges VCC pin.

Once the VCC voltage exceeds  $V_{CC\_Startup}$ , the JW7726B exits the UVLO. If VCC is lower than  $V_{CC\_UVLO}$ , the external MOSFET is turned off. The current flows through body diode before the VCC reaches to the startup voltage  $V_{CC\_startup}$ .

### Under-Voltage Lockout (UVLO)

When the VCC is below UVLO threshold, the external MOSFET is turned off and pulled low internally. Once the VCC exceeds the startup voltage  $V_{CC\_startup}$ , the parts is activated again.

### Turn On Phase

There are two conditions for the JW7726B to turn on the SR, i.e.  $V_{sw}$ , voltage-second value on SW pin when primary side switch is on, and the turn on phase is shown in Fig. 1.

1)  $V_{sw}$ : when the synchronous MOEFET is conducting, current flows through the body diode of MOSFET, which generates a negative voltage  $V_{SW}$  across it. When  $V_{SW}$  is lower than  $V_{MOS\_ON}$ , the part will pull the gate high to turn on the synchronous MOSFET after turn on delay time  $T_{DON}$  if the other condition is met.

2) Volt-second of SW: in DCM and QR operation, there are parasitic oscillations. In some applications, the drain resonant voltage may fall below the SR turn on threshold, especially for the first couple rings. SR could be falsely turned on, which may cause shoot through issue and result in high power loss. The volt-second value of SW pin can be used to distinguish the parasitic ring from normal primary side switch on. The threshold can be set by the resistance at VT pin. The curve is shown in Fig. 2.

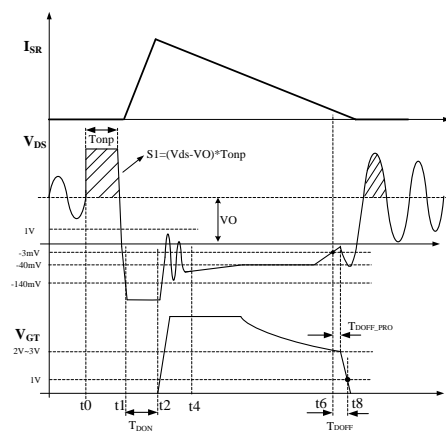


Fig. 1 Turn on delay and turn off delay

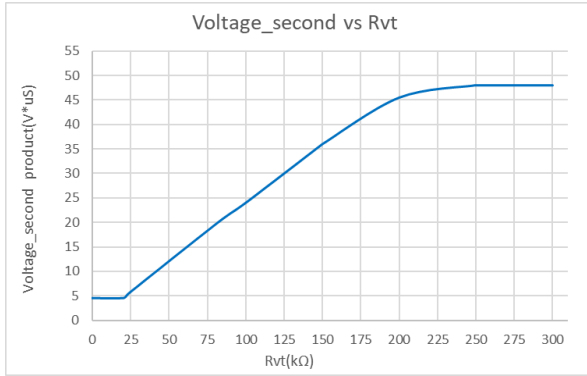


Fig. 2 Volt-second value vs. VT resistance

**Minimum On Time (MOT)**

When the synchronous MOSFET is turn on, there is a minimum on time for the SR. The  $V_{sw}$  voltage may have a parasitic ring when the synchronous MOSFET turns on. So, a minimum on time (MOT) is very important to avoid the MOSFET turn off threshold is false triggered. Minimum on time is 560ns for high frequency applications.

**Conducting Phase**

When the synchronous MOSFET is turned on, the drain source voltage  $V_{sw}$  it is determined by its on resistance and the current through it. The part adjusts the gate voltage and regulates the  $V_{sw}$  to the internal threshold (typical -40mV) after the synchronous MOSFET turn on. When

the  $V_{sw}$  is lower than -40mV, the gate keeps its maximum voltage. And the synchronous MOSFET is fully on.

The  $V_{sw}$  rises when the current follow through the MOSFET decreases. The gate voltage will be decreased to increase its on resistance and regulate the  $V_{sw}$  around -40mV.

It should be noted that the typical regulation threshold (-40mV) during MOSFET on time is not fixed, it can be internally changed to ensure the proper operation under CCM mode.

**Turn Off Phase**

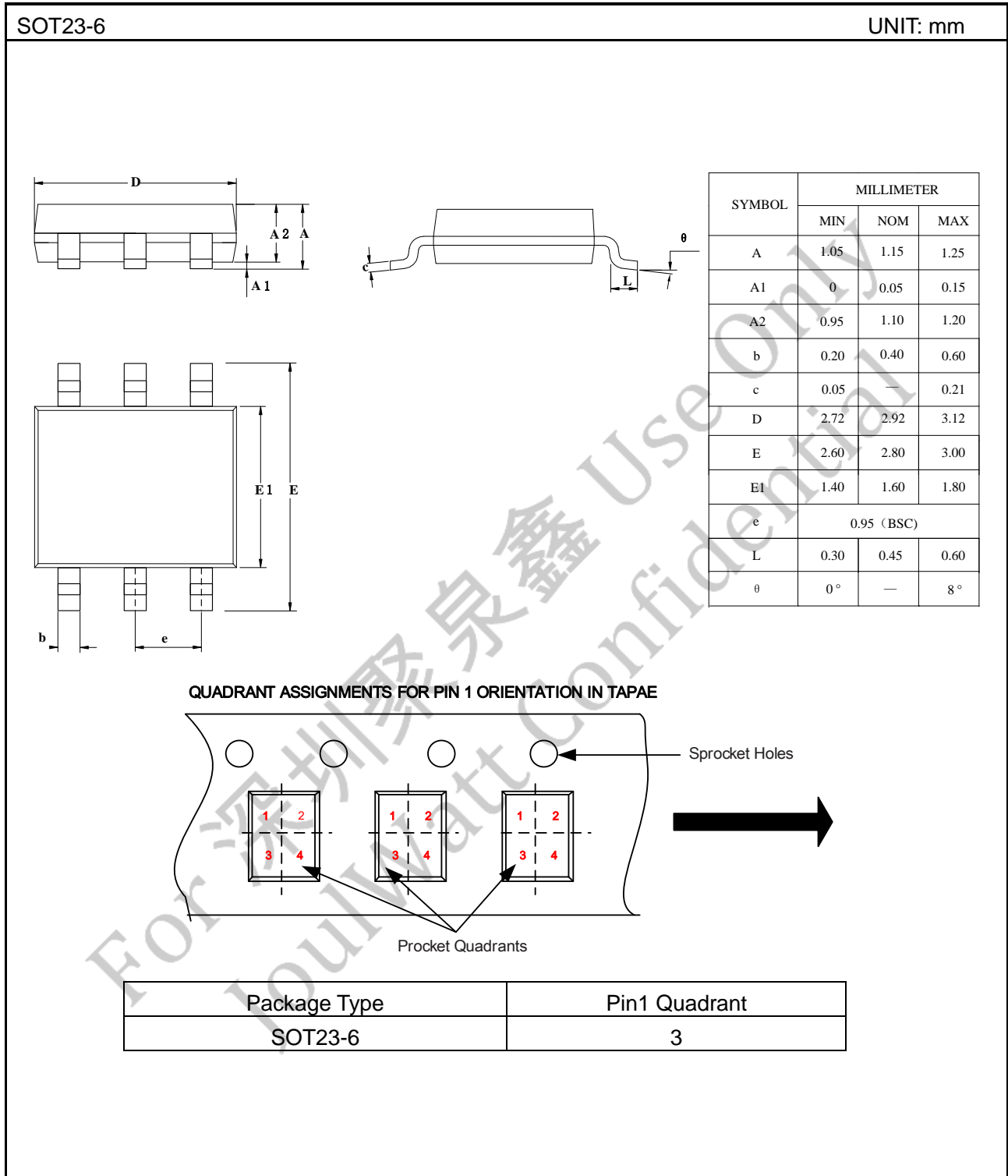
After synchronous MOSFET conducting, once the voltage  $V_{sw}$  touches the MOSFET turn off threshold (-3mV), the gate is pulled to low after a turn off delay time  $T_{DOFF}$ . A 330nS blanking time is necessary to avoid error trigger. The banking time is reset once  $V_{sw}$  rises above 2.5V.

**Output Voltage Detection**

The JW7726B has output voltage detection function via VO pin. VCC is charged from VO pin when VO is higher than 4.6V to save power loss caused by the LDO when charging from SW pin to VCC pin. When VO drops below 4.5V, the JW7726B is powered from SW pin.



PACKAGE OUTLINE



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