# JW5262N/JW5262NM

## 2A, 6V, 1.5MHz, 40uA $I_Q$ Synchronous Step-Down Converter

*Preliminary Specifications Subject to Change without Notice*

## DESCRIPTION

The JW5262N and JW5262NM are monolithic buck switching regulators based on constant on-time (COT) control for fast transient response. Operating with an input range of 2.6V-6.0V, the JW5262N & JW5262NM deliver 2A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency. At light loads, JW5262N and JW5262NM operate in low frequency to maintain high efficiency.

The JW5262N and JW5262NM guarantee robustness with hiccup output short-circuit protection, start-up current run-away protection and input under voltage lockout, and thermal protection.

The JW5262N and JW5262NM are available in 5-pin SOT23-5 and 6-pin SOT23-6 package, which provides a compact solution with minimal external components.



## FEATURES

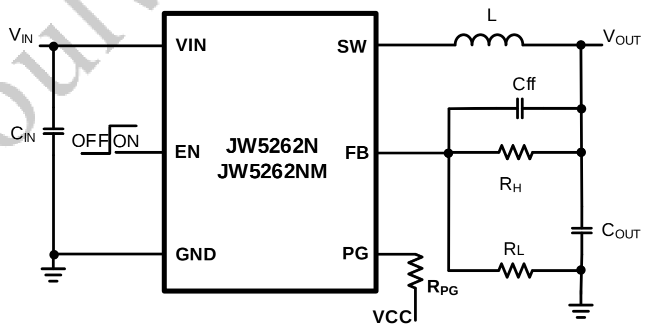
- 2.6V to 6.0V Operating Input Range
- Up to 2A Output Current
- Up to 92% Peak Efficiency
- PFM Mode at Light Load
- Internal Soft-start
- 1.5MHz Switching Frequency
- Input Under Voltage Lockout
- Current Run-away Protection
- Short Circuit Protection
- Thermal Protection
- Available in SOT23-5 and SOT23-6 Package

## APPLICATIONS

- 5V or 3.3V Point of Load Conversion
- Set Top Boxes
- Telecom/Networking Systems
- Storage Equipment
- GPU/DDR Power Supply



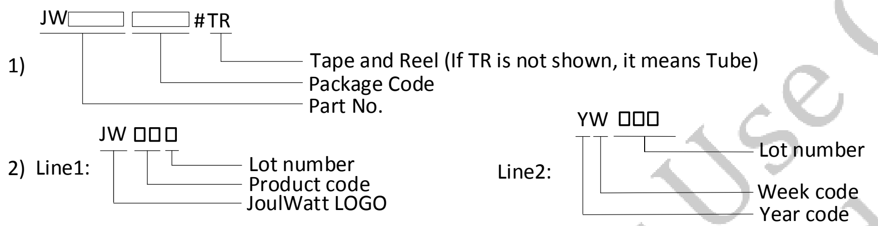
## TYPICAL APPLICATION



## ORDER INFORMATION

| DEVICE[1] | PACKAGE | TOP MARKING[2] | ENVIRONMENTAL[3] |
|---|---|---|---|
| JW5262NSOTA#TR | SOT23-5 | JWTJ□<br>YW□□□ | Green |
| JW5262NSOTB#TR | SOT23-6 | JWTJ□<br>YW□□□ | Green |
| JW5262NMSOTA#TR | SOT23-5 | JWTH□<br>YW□□□ | Green |

**Notes:**

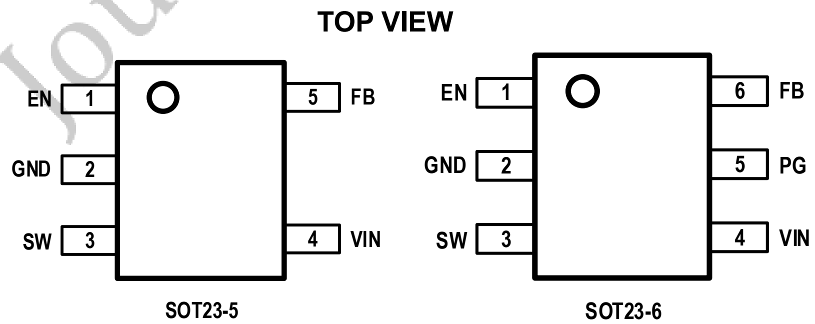



3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

## DEVICE INFORMATION

| DEVICE[1] | Operation Mode at light load | Function | Package | MSL |
|---|---|---|---|---|
| JW5262NSOTA#TR | PFM | - | SOT23-5 | MSL1 |
| JW5262NSOTB#TR | PFM | PG | SOT23-6 | MSL1 |
| JW5262NMSOTA#TR | PFM | - | SOT23-5 | MSL3 |

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATING[1)]

Vin, EN, FB, PG Pins ........................................................................................................-0.3V to 7.0V
SW Pin ….......................................................-0.3V(-1V for 20ns, -3V for 10ns) to 7.0V(9.5V for 10ns)
Junction Temperature [2)] ..........................................................................................................150ºC
Lead Temperature…..................................................................................................................260ºC
Storage Temperature ......................................................................................... -65ºC to +150ºC
ESD Susceptibility (Human Body Model) ........................................................................... 2kV

## RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage $V_{IN}$ ........................................................................................................2.6V to 6.0V
Output Voltage $V_{OUT}$.........................................................................................................0.6V to $V_{IN}$ V
Operating Junction Temperature.............................................................................-40ºC to 125ºC

## THERMAL PERFORMANCE[4)]

| | $\theta_{JA}$ | $\theta_{Jc}$ |
|---|---|---|
| SOT23-5 | 220 | 110ºC/W |
| SOT23-6 | 220 | 110ºC/W |

**Note：**

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
2) The JW5262N & JW5262NM include thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

*VIN=5V, $T_A$=25 ℃, unless otherwise stated.*

*Advance Information, not production data, subject to change without notice.*

| Item | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ Under Voltage Lockout Threshold | $V_{IN\_UVLO}$ | $V_{IN}$ rising | | 2.3 | 2.45 | V |
| $V_{IN}$ Under Voltage Lockout Hysteresis | $V_{IN\_UVLO\_HYST}$ | $V_{IN}$ falling | | 200 | | mV |
| EN Rising Threshold | $V_{EN\_H}$ | $V_{EN}$ rising, FB=0.3V | 1.1 | 1.2 | 1.3 | V |
| EN Falling Threshold | $V_{EN\_L}$ | $V_{EN}$ falling, FB=0.3V | 0.9 | 1 | 1.1 | V |
| EN delay time[5] | $t_{EN\_delay}$ | | | 290 | | uS |
| Shutdown Current | $I_{SHDN}$ | $V_{IN}$=6.0V, $V_{EN}$=0V | | 0.1 | 1 | μA |
| Quiescent Current | $I_Q$ | $V_{EN}$=5V, $I_{OUT}$=0A, $V_{FB}$=$V_{REF}$*105% | | 40 | 70 | μA |
| Regulated Feedback Voltage | $V_{FB}$ | 2.6V<$V_{IN}$<6.0V | 0.594 | 0.6 | 0.606 | V |
| | | $T_j$=-40 ℃~125 ℃ | 0.588 | 0.6 | 0.612 | V |
| FB Leakage Current | $I_{FB}$ | $V_{FB}$=0.7V | | | 100 | nA |
| PFET On Resistance[5] | $R_{DSON\_P}$ | | | 120 | | mΩ |
| NFET On Resistance[5] | $R_{DSON\_N}$ | | | 90 | | mΩ |
| PFET Leakage Current | $I_{LEAK\_P}$ | $V_{IN}$=6.0V, $V_{EN}$=0V, $V_{SW}$=0V | | | 1 | uA |
| NFET Leakage Current | $I_{LEAK\_N}$ | $V_{IN}$=6.0V, $V_{EN}$=0V, $V_{SW}$=6.0V | | | 1 | uA |
| PFET Current Limit | $I_{LIM\_TOP}$ | | | 4 | | A |
| NFET Current Limit | $I_{LIM\_BOT}$ | | 2 | 2.5 | 3 | A |
| Switch Frequency | $F_{SW}$ | CCM | | 1.5 | | MHz |
| Minimum On Time | $T_{ON\_MIN}$ | | | 100 | | ns |
| Minimum Off Time | $T_{OFF\_MIN}$ | | | 80 | | ns |
| Maximum Duty Cycle[5] | $D_{MAX}$ | | | 100 | | % |
| Soft-Start Period | $t_{SS}$ | 10% to 90% $V_{ref}$ | | 1 | | ms |
| Discharge Resistance | $R_{DISC}$ | | | 1 | | KΩ |
| Power Good Threshold | $V_{PG\_H}$ | $V_{FB}$ rising, referenced to $V_{FB}$ nominal (SOT23-6) | | 95% | | |
| | $V_{PG\_L}$ | $V_{FB}$ falling, referenced to $V_{FB}$ nominal (SOT23-6) | | 90% | | |
| Power Good Deglitch time | $T_{PG\_Delay}$ | (SOT23-6) | | 40 | | us |
| Low-level output voltage at PG pin | $V_{PG\_OL}$ | $I_{PG}$= 1 mA (SOT23-6) | | | 0.4 | V |
| Thermal Shutdown Threshold[5] | $T_{SHDN}$ | | | 150 | | ℃ |

*VIN=5V, $T_A$=25℃, unless otherwise stated.*
*Advance Information, not production data, subject to change without notice.*

| Item | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Shutdown Hysteresis | $T_{HYST}$ | | | 20 | | ℃ |

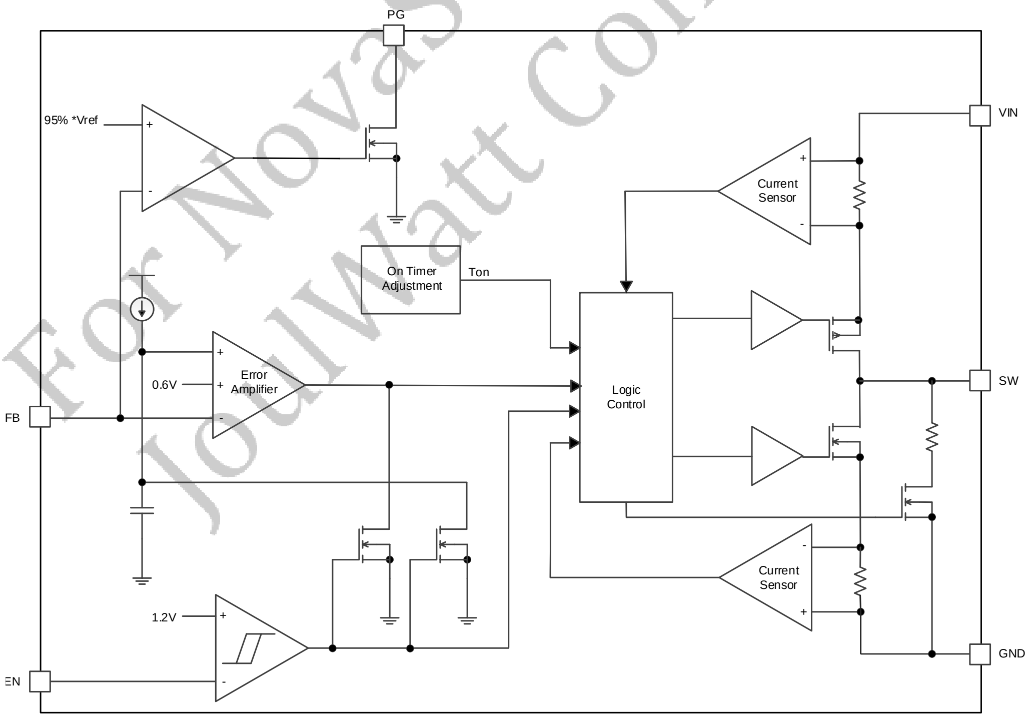
**Note:**

**5)** Guaranteed by design.

## PIN DESCRIPTION

| Pin SOT23-6 | Pin SOT23-5 | Name | Description |
|---|---|---|---|
| 1 | 1 | EN | Drive EN pin high to turn on the regulator and low to turn off the regulator. |
| 2 | 2 | GND | Ground pin. |
| 3 | 3 | SW | SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. |
| 4 | 4 | VIN | Input voltage pin. VIN supplies power to the IC. Connect a 2.6V to 6.0V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. |
| 5 | | PG | Open drain output. Connect a 10KΩ resistor from PG to VIN. If it's not used, leave the pin floating. |
| 6 | 5 | FB | Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB. |

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

The JW5262N and JW5262NM are constant on-time control, synchronous, step-down regulators. They regulate input voltages from 2.6V~6.0V down to an output voltage as low as 0.6V, and are capable of supplying up to 2A of load current.

### Constant On-time Control

The JW5262N and JW5262NM utilize constant on-time control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier.
Output of the internal error amplifier is compared with the switch current measured internally to control the output current limit.

### PFM Mode

The JW5262N and JW5262NM operate in PFM mode at light load. In PFM mode, switch frequency is continuously controlled in proportion to the load current, i.e. switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

### Shut-Down Mode

The JW5262N and JW5262NM operate in shut-down mode when voltage at EN pin is driven below 0.4V. In shut-down mode, the entire regulator is off and the supply current consumed by the IC drops below 1uA.

### Power Switches

P-channel and N-channel MOSFET switches are integrated on the JW5262N and JW5262NM to down convert the input voltage to the regulated output voltage.

### 100% Duty Cycle Low Dropout Operation

The devices offer low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain output regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times R_{DR}$$

Where

$V_{IN\_MIN}$ is the minimum input voltage to maintain an output voltage;

$I_{OUT\_MAX}$ is the maximum output current;

$R_{DR}$ is the high-side MOSFET on-resistance and the inductor conductive resistance in series.

To enter 100% duty cycle mode, when the input voltage gradually approaches the output voltage, the off time of the high-side MOSFET will reach min off time (typically 80ns) and the switching frequency is reduced to maintain output voltage. At this condition, the high-side MOSFET will be forced off when the inductor current reaches 2.3A.

### Short Circuit Protection

When output is shorted to ground, the switching frequency is reduced to prevent the inductor current from increasing beyond PFET current limit. If short circuit condition holds for more than 1024 cycles, both PFET and NFET are forced off and can be enabled again after 4ms. This procedure is repeated as long as short circuit condition is not removed.

### Power Good（SOT23-6）

JW5262N has built in power good (PG) function to indicator whether the output voltage has reached its appropriate level or not. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG signal can be used for startup sequencing for multiple rails. The PG pin is an open drain output. JW5262N features PG=Low when the device is turned-off due to EN=Low, UVLO and thermal shutdown.

### Thermal Protection

When the temperature of the IC rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 130°C can the regulator becomes active again.

# APPLICATION INFORMATION

## Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_L}{R_L + R_H}$$

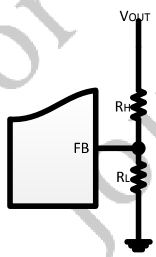
where $V_{FB}$ is the feedback voltage and $V_{OUT}$ is the output voltage.

Choose $R_L$ around 10kΩ, and then $R_H$ can be calculated by:

$$R_H = R_L \cdot \left( \frac{V_{OUT}}{0.6} - 1 \right)$$

The following table lists the recommended values.

| $V_{OUT}$ (V) | $R_L$(kΩ) | $R_H$(kΩ) |
|---|---|---|
| 0.8 | 12 | 4 |
| 1 | 30 | 20 |
| 1.2 | 10 | 10 |
| 1.8 | 10 | 20 |
| 3.3 | 11 | 49.9 |




## Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. Estimate the RMS current in the input capacitor with:

$$I_{CIN} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where $I_{LOAD}$ is the load current, $V_{OUT}$ is the output voltage, $V_{IN}$ is the input voltage.

The input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where $C_{IN}$ is the input capacitance value, fs is the switching frequency, $\Delta V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors.

10uFx2 ceramic capacitors are recommended in typical application.

## Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left( R_{ESR} + \frac{1}{8 \cdot fs \cdot C_{OUT}} \right)$$

where $C_{OUT}$ is the output capacitance value and $R_{ESR}$ is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and 22uF ~ 22uFx2 ceramic capacitors are recommended in typical application.

## Inductor Selection

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

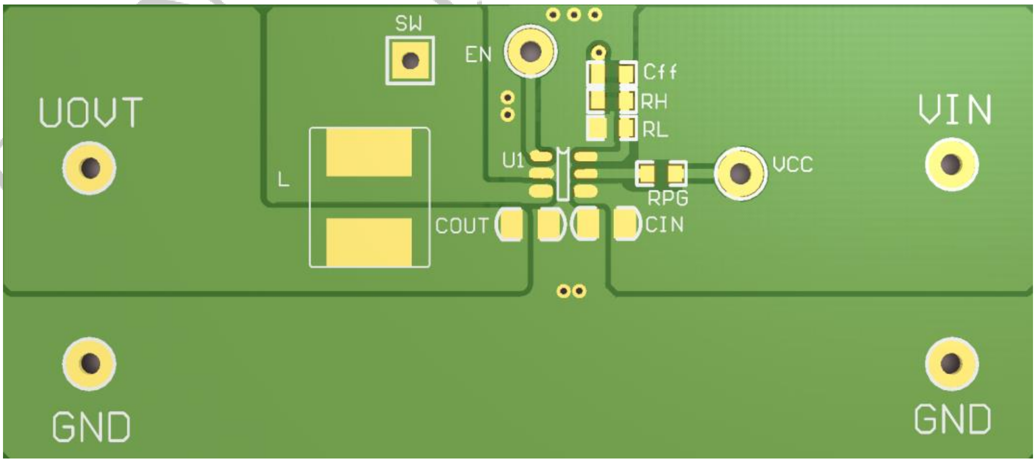
where $V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage, $f_S$ is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

## PCB Layout Guidelines

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5262N or JW5262NM ($V_{IN}$ pin and GND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.
4. Keep the switching node SW short to prevent excessive capacitive coupling.
5. Make $V_{IN}$, $V_{OUT}$ and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

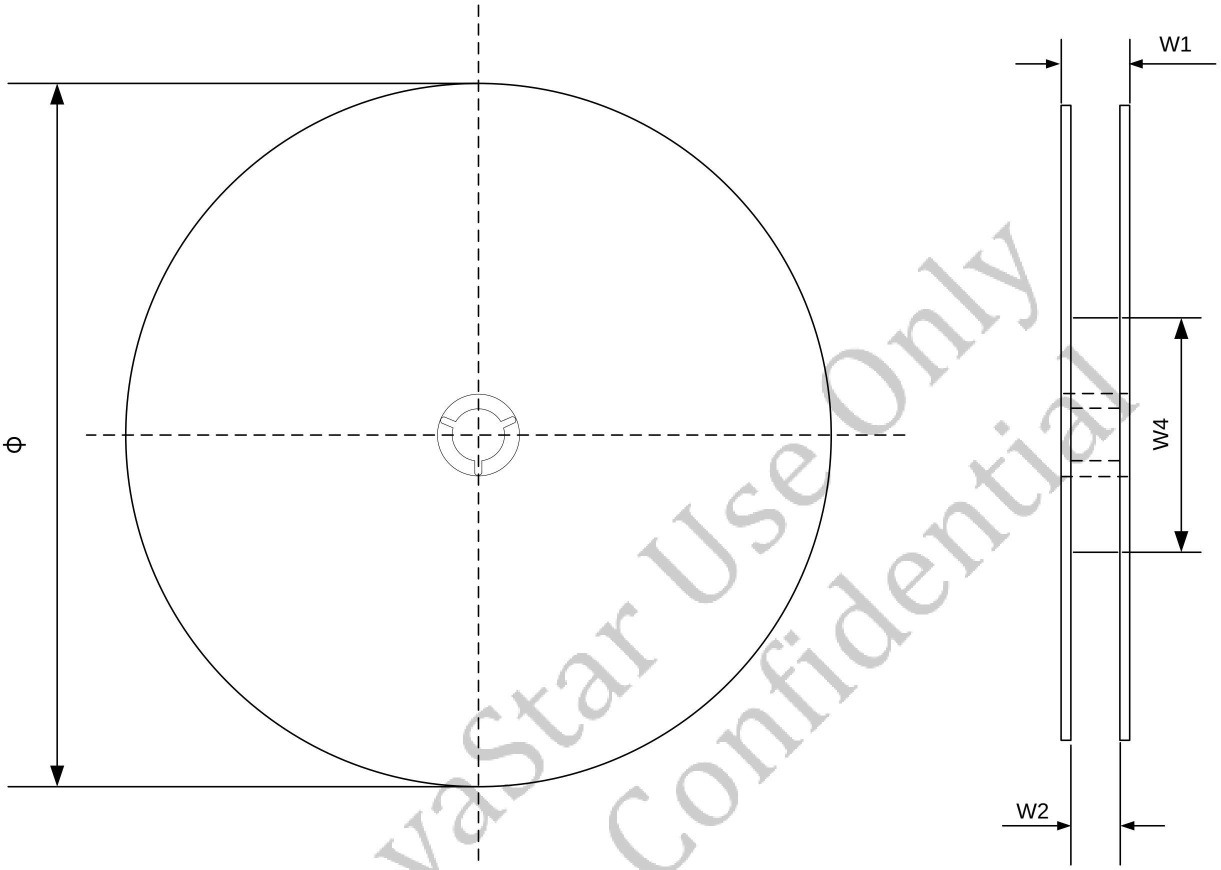
SOT23-6:




PCB Layout Recommendation

## TAPE AND REEL INFORMATION

Reel UNIT: mm

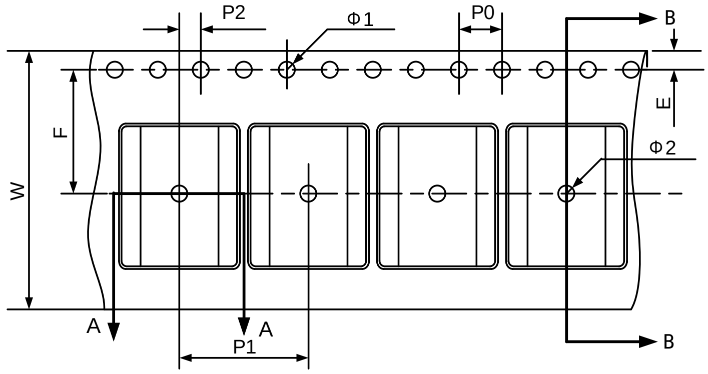


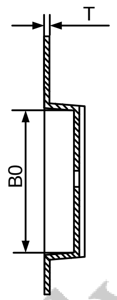



| Package | Diameter Φ | Thickness W1 | Width W2 | W4 |
|---|---|---|---|---|
| SOT23-5(6) | 178±2 | 12.30±2 | 9.5±2 | 58±4 |

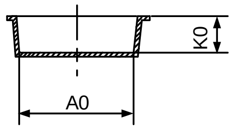
## Carrier Tape

UNIT: mm




SECTION B-B




SECTION A-A

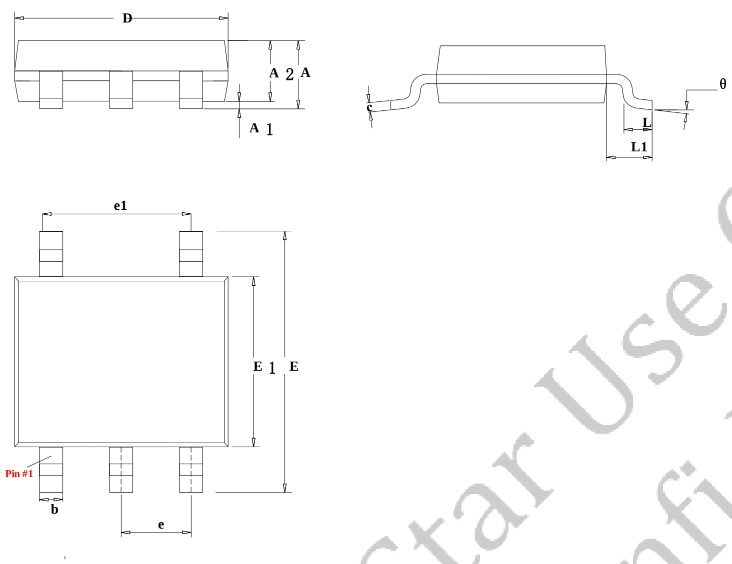
Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

| Package | Tape dimensions（mm） | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | P0 | P2 | P1 | A0 | B0 | W | T | K0 | Φ1 | Φ2 | E | F |
| SOT23-5(6) | 4.0±0.1 | 2.0±0.1 | 4.0±0.1 | 3.23±0.2 | 3.13±0.3 | 8.0±0.3 | 0.25±0.2 | 1.37±0.2 | 1.55±0.15 | 1.00min | 1.75±0.1 | 3.50±0.1 |

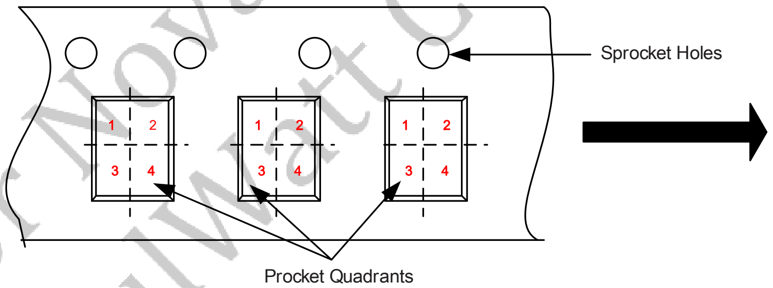
# PACKAGE OUTLINE

SOT23-5 UNIT: mm



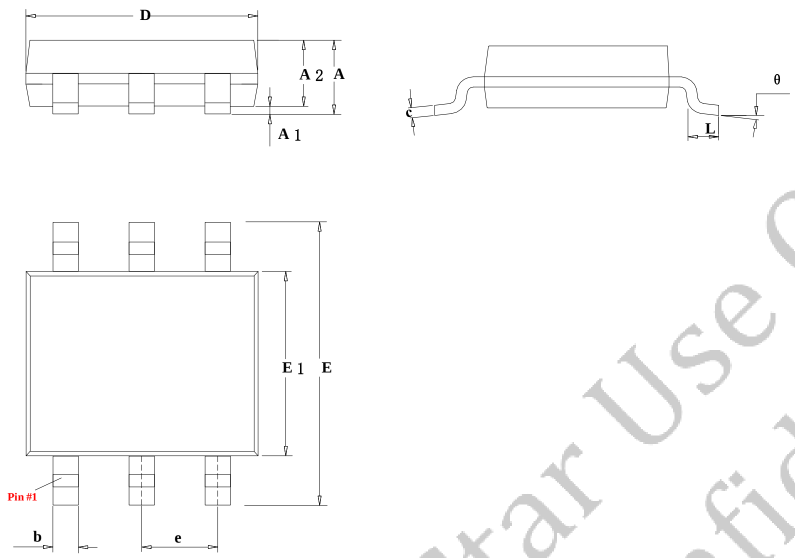

| SYMBOL | MILLMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.35 |
| A1 | 0 | — | 0.15 |
| A2 | 1.00 | 1.10 | 1.20 |
| b | 0.30 | — | 0.50 |
| c | 0.10 | — | 0.22 |
| D | 2.82 | — | 3.02 |
| E | 2.60 | — | 3.00 |
| E1 | 1.41 | — | 1.72 |
| e | 0.95(BSC) | | |
| L | 0.30 | — | 0.60 |
| θ | 0° | — | 8° |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



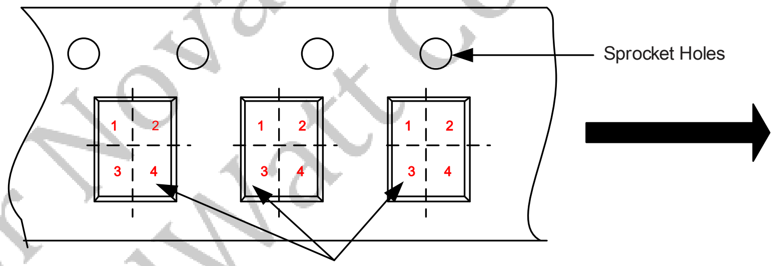

| Package Type | Pin1 Quadrant |
|---|---|
| SOT23-5 | 3 |

SOT23-6 UNIT: mm




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | -- | 1.35 |
| A1 | 0 | -- | 0.15 |
| A2 | 1.00 | 1.10 | 1.20 |
| b | 0.30 | -- | 0.50 |
| c | 0.10 | -- | 0.22 |
| D | 2.82 | -- | 3.02 |
| E | 2.60 | -- | 3.00 |
| E1 | 1.41 | -- | 1.72 |
| e | 0.95（BSC) | | |
| L | 0.30 | -- | 0.60 |
| θ | 0° | -- | 8° |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




| Package Type | Pin1 Quadrant |
|---|---|
| SOT23-6 | 3 |

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