JW1566A

Offline QR GaN Flyback Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®1566A is an isolated offline Flyback converter with GaN integrated, which features quasi-resonant (QR) operation. QR control improves efficiency by reducing switching loss and benefits EMI performance with nature frequency variation, and an internal maximum frequency limitation to overcome the inherent disadvantages of QR Flyback.

The JW1566A combines PWM and PFM control at different input and load condition for highest average efficiency. It can comply with the most stringent efficiency regulations.

The JW1566A is both available in DFN5X6-7 package. The high level of integration results in a simple to use, low component count, and high efficiency application solution for isolated power delivery.

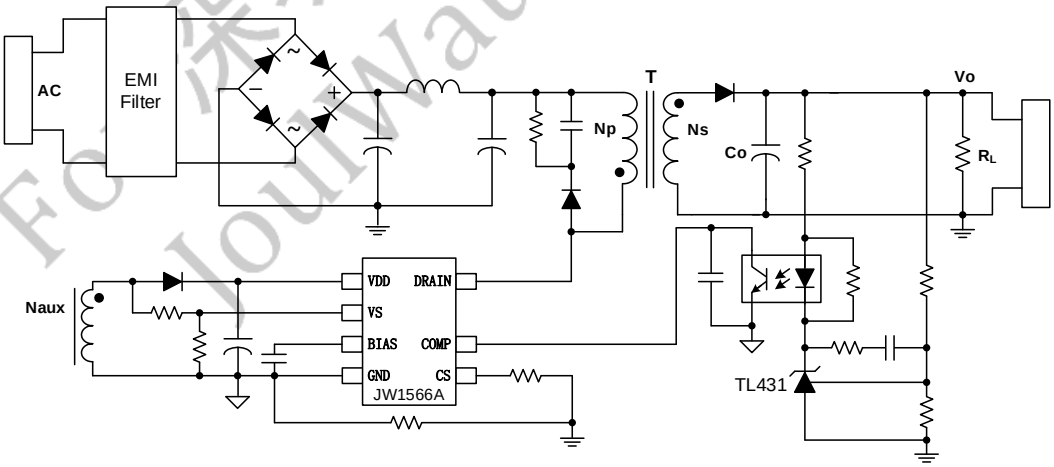
FEATURES

- Integrated 650V 480mΩ GaN
- Wider VDD Operation Range (Up to 90V)
- QR Operation for High Efficiency
- Maximum 260kHz Switching Frequency
- Optional OCP and OPP Function for Different PD and QC Output Application
- Very Low Standby Power Consumption
- Cycle-by-Cycle Current Limit
- Reliable Fault Protections: VDD OVP, VS OVP and UVP, Brown-In, CS Open Protection, OCP, OPP, Internal OTP
- Frequency Jitter to Ease EMI Compliance
- DFN5X6-7 Package

APPLICATIONS

- PD and Quick-Charging Chargers
- AC/DC Adapters with Wide Output Range

TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW1566ADFNY#TR	DFN5X6-7	JW1566A YW□□□□□	Green

Notes:

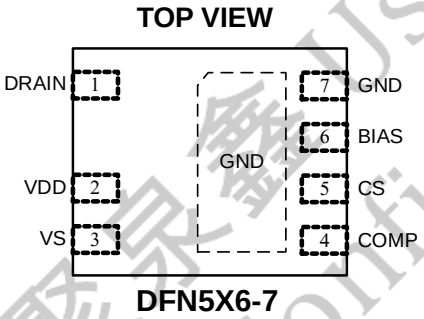
1) JW□□□□#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

2) Line1: JW □□□□
- Product code
- Joulwatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



DFN5X6-7

ABSOLUTE MAXIMUM RATING[1)]

DRAIN Pin 650V
VDD Pin 100V
COMP, CS Pin .....-0.3V to 5V (5V to 5.5V<10us)
BIAS Pin .....-0.3V to 6.3V (6.3V to 7V<10us)
VS Pin .....-0.3V to 5V (-0.7V to -0.3<10us, 5V to 5.5V<10us)
Junction Temperature[2) 3)] 150ºC
Storage Temperature ..... -65ºC to 150ºC
Lead Temperature (Soldering, 10sec.) 260ºC
Continuous Power Dissipation (TA = +25 ºC) [4)] DFN5*6..... 2.5W

RECOMMENDED OPERATING CONDITIONS

VDD Voltage ..... 8V to 88V
Operating Junction Temperature (T_J) ..... -40ºC to 125ºC

THERMAL PERFORMANCE[5)]

	θ_{JA}	θ_{Jc}
DFN5x6-7	50	3ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress rating do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW1566A includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA.

5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_A = 25ºC, unless otherwise stated.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage Section *(VDD Pin)*						
Turn-On Threshold Voltage	V_{DD_ON}	VDD Rising	15.1	16.3	17.6	V
Turn-Off Threshold Voltage	V_{DD_OFF}	VDD Falling	6.8	7.4	8	V
Reset Threshold Voltage	V_{DD_RST}		3.8	4.7	5.6	V
VDD Charging Current	I_{DD_CHG}		2.5	3	3.5	mA
Startup Current	I_{DD_ST}	VDD=V_{DD_ON}-0.5 V,		300		uA
Operating Supply Current	I_{DD_OP}	VDD=20V, fs=260kHz		0.9		mA
VDD OVP Voltage	V_{DD_OVP}		85	90	95	V
Voltage Sense Section *(VS Pin)*						
Maximum VS Source Current Capability	I_{VS_MAX}		2.3	2.9	3.5	mA
Output OVP Threshold	V_{VS_OVP}		2.8	3	3.2	V
Output UVP Threshold	V_{VS_UVP}		0.2	0.25	0.3	V
Adaptive Blanking Time for VS Sampling[6)]	t_{VS_BLK}	COMP=0.5V		0.6		us
		COMP=3.6V		2		us
Output OVP Debounce Cycle Counts[6)]	N_{VS_OVP}			3		Cycle
Output UVP Blanking Time	t_{VS_UVP}		89.5	106	122.5	ms
Auto-Restart Cycles for UVP[6)]	N_{UVP_HIC}			4		Cycle
Current Sense Section *(CS Pin)*						
Max CS Offset Current	I_{CS_MAX}	VDD=20V, COMP=3.6V	96	100	104	uA
Min CS Offset Current	I_{CS_MIN}	VDD=20V, COMP=0.5V at Burst Mode	21	27	33	uA
CS Off Threshold	V_{CS_TH}			31	65	mV
Leading-Edge Blanking Time	t_{LEB}			150		ns
OCP Enable Threshold	V_{OCP_EN}		0.5	0.65	0.8	V
OCP Blanking Time	t_{OCP_BLK}		89.5	106	122.5	ms
OCP Internal Threshold[6)]	V_{OCP}		0.19	0.2	0.21	V
Auto-Restart Cycles for OCP[6)]	N_{OCP_HIC}			4		Cycle
Frequency Section						
Maximum Switching Frequency	f_{max}		220	260	300	kHz
Minimum Switching Frequency	f_{min}		20	25	30	kHz
Maximum ON Time	T_{ON_MAX}		15	19	23	us
Minimum ON Time	T_{ON_MIN}		150	195	240	ns
Maximum Switching Cycle	T_{S_MAX}		52	61.5	71	us

Frequency Jittering Amplitude to COMP[6)]	ΔF_{JIT}			±7%		
Counting Cycles for Jittering[6)]	N_{JIT_CYC}			32		Cycle
Feedback Section *(COMP Pin)*						
Open Pin Voltage[6)]	V_{COMP_MAX}	Open Loop		4.0		V
Internal Pull-Up Resistor[6)]	R_{COMP_UP}			20		kΩ
COMP to CS Offset Current Gain	G_{COMP_CS}	COMP > 2.8V		20		V/mA
		COMP < 1.0V		16		V/mA
The Threshold Enter PFM Mode	V_{COMP_PFM}			2.8		V
The Threshold Enter Burst Mode	V_{BUR_L}		0.4	0.5	0.6	V
The Threshold Exit Burst Mode	V_{BUR_H}		0.54	0.6	0.66	V
OPP Blanking Time	t_{OPP_BLK}		89.5	106	122.5	ms
OPP Internal Threshold[6)]	V_{OPP}		0.76	0.8	0.84	V
Auto-Restart Cycles for OPP[6)]	N_{OPP_HIC}			4		Cycle
Over Load Protection Threshold	V_{OLP}			3.6		V
OLP Blanking Time	t_{OLP_BLK}		89.5	106	122.5	ms
Auto-Restart Cycles for OLP[6)]	N_{OLP_HIC}			4		Cycle
GaN Section						
Drain-source On-state Resistance	R_{DS_ON}			500		mΩ
Brown-In Threshold	V_{BR_IN}		103	111	119	V
Rising Time[6)]	t_r			50		ns
Falling Time[6)]	t_f			30		ns
Internal Over Temperature Protection						
Thermal Shutdown Threshold[6)]	T_{OTP}			140		°C
OTP Hysteresis[6)]	T_{HYS}			30		ºC

Note:

6) Guaranteed by design.

PIN DESCRIPTION

Pin DFN5X6-7	Name	Description
1	DRAIN	Drain terminal of the Internal GaN.
2	VDD	Bias power input to the controller. A hold-up capacitor to GND is required.
3	VS	Voltage sensing input pin. Coupled to the auxiliary winding via a resistor divider to monitor the output voltage for OVP and UVP protection. This pin also detects the resonant valley to implement QR operation.
4	COMP	Feedback input pin for Flyback QR controller. Connect to an opto-coupler directly.
5	CS	Current sensing input pin. This pin sense the primary switch current for peak current control and OCP. Besides, this pin is used to choose OCP or OPP at the initial start.
6	BIAS	Bias power of the driver, an external hold-up capacitor to GND is required
7	GND	The ground of the IC.
--	NC	

BLOCK DIAGRAM

TBD

FUNCTIONAL DESCRIPTION

The JW1566A is an offline flyback converter with GaN intergrated, which features multi-mode quasi-resonant (QR) operation. The Quasi- Resonant (QR) with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

JW1566A has an inherent frequency jittering mechanism to improve the EMI performance under QR operation.

1. Start-Up

1.1. High Voltage Start-Up at Drain Terminal

An internal high voltage startup circuit is connected to the drain terminal of the GaN, the internal JFET turns on and a current source starts to charge VDD cap. As soon as VDD reaches turn-on threshold V_{DD_ON} (16.5V), the internal startup circuit is disabled. The controller is enabled and the converter starts switching. The VDD turn-off threshold (V_{DD_OFF}) is 7.5V.

1.2 Soft-Start

In the absence of a detected fault, the controller begins to work normally along with soft start. The internal soft-start time is within 3 ms with the feedback signal V_{COMP} rising gradually from the minimum level to the maximum level. Every restart up is followed by a soft start.

2. Normal Operation

After the controller start-up, it enters normal operation. The JW1566A realizes the output adjustment based on the feedback signal transmitting to the primary-side controller by the opto-coupler.

JW1566A is a multi-mode QR converter with secondary-side regulation. According to the feedback signal V_{COMP}, the converter operates in different modes for efficiency optimization. Fig.1 illustrates the frequency and peak current amplitude modulation modes. It can be divided into four operation regions as shown in Fig.1.

Under heavy load condition, the system operates in QR mode, the maximum switching frequency is limited to 260kHz. For medium-load range, the Pulse Frequency Modulation (PFM) is used and primary peak current is nearly fixed to achieve high efficiency. When the load is further reduced, switching frequency is fixed at 25kHz along with primary peak current varying from 50% to 25% of its maximum. When the system is at very light load condition, the control mode of JW1566A changes to burst mode. When the voltage of COMP pin drops below V_{BUR_L} (0.5V), the drive stops. The drive will resume when the voltage of COMP pin rises back to V_{BUR_H} (0.6V). Otherwise the GaN remains at off state to minimize the switching loss and reduce the standby power consumption. Transitions between modes are automatically accomplished by the controller depending on the feedback signal, V_{COMP}.

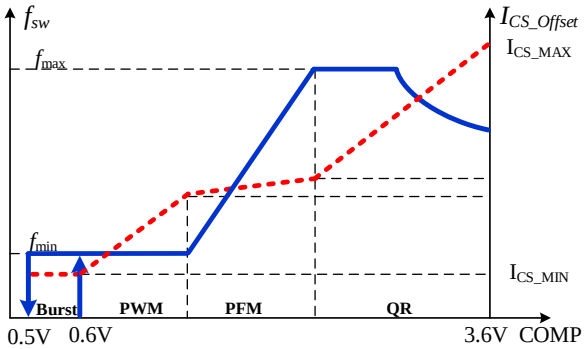


Fig.1 Frequency & Ipk Modulation

3. Other Functions and Features

3.1 Frequency Jittering

To achieve good EMI performance, frequency jittering method is integrated in JW1566A. The frequency jittering is achieved by varying the switching frequency directly. The variation is ±7% around its normal value. The modulation cycle is determined by counting consecutive 32 switching cycles.

3.2 Lead Edge Blanking (LEB)

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) is used between the CS pin and the current comparator input. The current comparator is disabled and can't turn off the internal GaN during the blanking time. The normal LEB time is around 150ns. Fig.2 shows the leading edge blanking time.

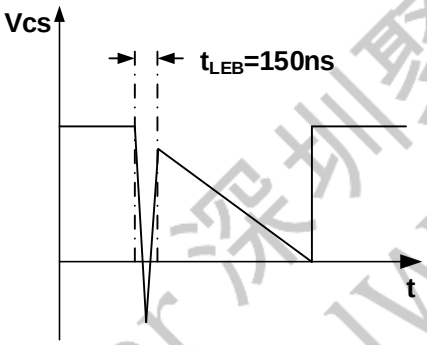


Fig.2 LEB Blanking

3.3 CCM Preventing

For JW1566A, when the primary-side peak current exceeds the value decided by the feedback signal V_{COMP}, the switch turns off. When the controller detects ZCD signal and the switch period exceeds frequency-limit signal, the switch turns on. But the ZCD signal may not be detected during start-up moment because of low output voltage, then the switch will turn on after a maximum switching cycle to make sure the system operates in DCM.

3.4 VS Blanking Time

VS spikes are affected by the amplitudes of Ipk and inductance, so VS blanking time should be set to vary with Ipk. Ensure that the secondary side conduction time is greater than the VS Blanking Time.

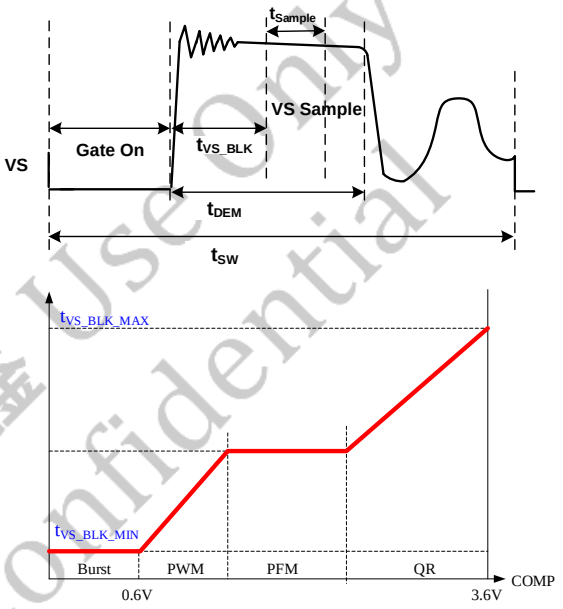


Fig.3 VS Blanking Time

4. Protection

4.1 CS Pin Open Protection

When CS pin is open, the internal bias current will flow to the parasitic capacitance on the CS pin, increasing the V_{CS}. If V_{CS} is above 2.0V, a CS pin open fault triggered.

4.2 Input Brown in

The JW1566A senses Drain voltage to realize brown in function. When Drain voltage is higher than V_{BR_IN} (112V typically), a 5mA pull down current will be applied to VDD pin to make VDD hit V_{DD_OFF}. When VDD reaches V_{DD_ON} again, the controller starts switching.

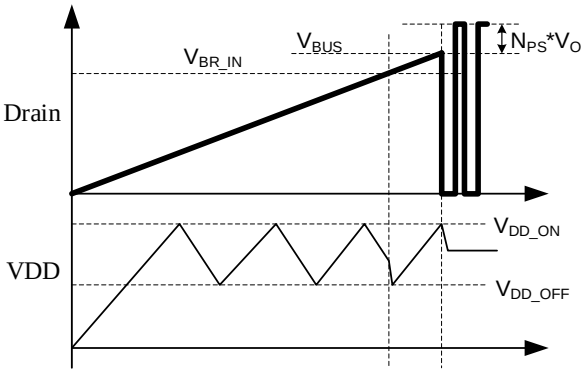


Fig.4 Brown-In at Drain Terminal

4.3 Output OVP (VS OVP)

The output over voltage protection is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 3V for three consecutive switching cycles, an VS_OVP fault is asserted, and then the device shuts down, the UVLO reset and re-start fault cycle begins.

4.4 VS UVP

If the voltage sample on VS pin continues below the under-voltage protection threshold (0.25V) more than 120ms, a VS_UVP fault is asserted. When a VS_UVP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.5 OCP or OPP Selection Circuit

In some PD or QC applications, the maximum output current at different output voltage differs much. So OCP should be disabled, and the alternative OPP is enabled. JW1566A senses CS voltage at initial start to determine whether to use OCP or OPP function as Fig.5 shows. At the initial 100us, a 100uA current is applied to CS pin. If CS voltage exceeds a preset enable threshold (typical 0.65V), OPP is enabled and OCP is disabled. Otherwise, OPP is disabled and OCP is enabled.

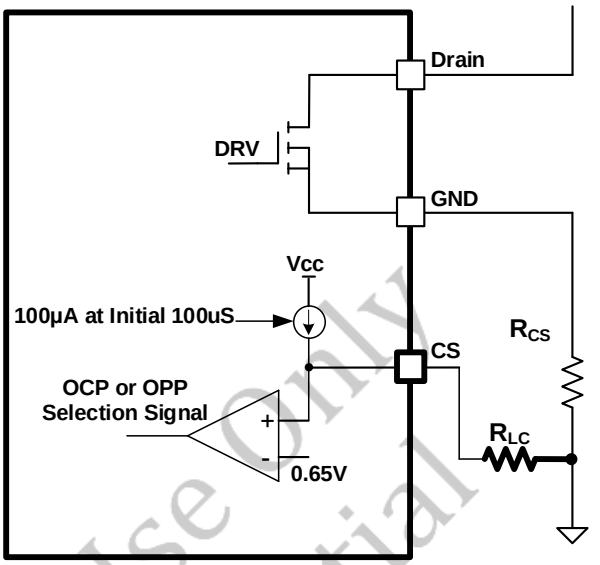


Fig.5 OCP or OPP Selection Circuit

4.6 OCP

If OCP is enabled, JW1566A compares estimated output average current and OCP threshold. The output average current is calculated at the primary side. When the primary switch turns off, the peak inductor current (I_{pk}) is sampled and hold for output current calculation.

As shown in Fig.6, it calculates output current based on secondary side current conduction time T_{ons} and primary side current information V_{CS}. If the calculated output current signal, I_{o_est} is higher than the internal OCP threshold V_{OCP} (0.2V typically) for 120ms (OCP blanking time), IC enters OCP protection.

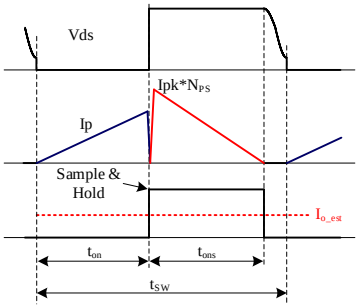


Fig.6 Output Current Estimation

So the OCP point can be set as:

$$I_o = \frac{V_{ocp} \cdot N_P}{2 \cdot R_{CS} \cdot N_S} \quad (1)$$

wherein, N_P is the turns number of primary winding, N_S is the turns number of secondary winding, R_{cs} is the current sensing resistance.

When an OCP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.7 OPP

If OPP is enabled, JW1566A compares estimated output power and OPP threshold. The output power is calculated at the primary side based on the estimated output average current in OCP and the output voltage according to VS voltage. So the output power can be expressed as:

$$P_{out} = I_o \cdot V_o = \frac{V_{CS\_PEAK} \cdot D_S \cdot N_P}{2 \cdot R_{CS} \cdot N_S} \cdot \frac{VS \cdot N_S}{N_{aux}} \cdot \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (2)$$

And the OPP point can be set as:

$$P_{out} = \frac{V_{OPP} \cdot N_P}{2 \cdot R_{CS} \cdot N_{aux}} \cdot \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (3)$$

wherein, N_{aux} is the turns number of auxiliary winding, N_P is the turns number of primary winding.

If the calculated output power signal is higher than the internal OPP threshold V_{OPP} (0.8V typically) for 120ms (OPP blanking timer), IC enters OPP protection. When an OPP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.8 Over Load Protection

If the voltage on COMP pin continues exceeds the Over-Load protection threshold (3.6V typically) more than 120ms, an OLP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

4.9 VDD OVP

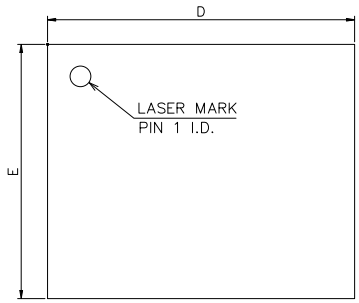
If the voltage on VDD pin continues exceeds the Over-Voltage protection threshold (90V typically) more than 100us, a VDD OVP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

4.10 Internal OTP

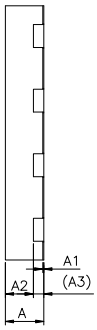
The internal over temperature protection threshold is 140°C. If the junction temperature of the device reaches this threshold, the device shuts down. When the junction temperature falls below 110°C, the device initiates the UVLO reset and re-starts fault cycle.

PACKAGE OUTLINE

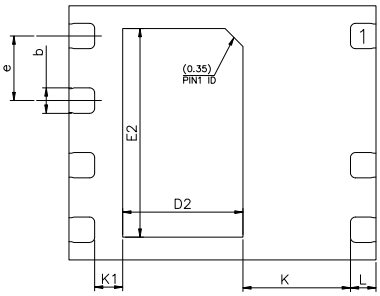
DFN5x6-7 Unit: mm



TOP VIEW



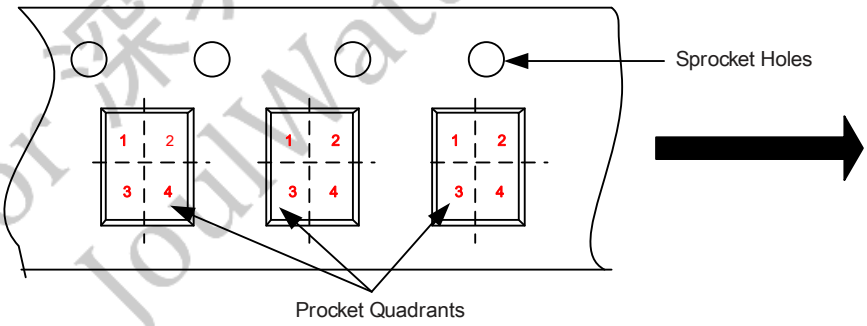
SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	—	0.55	—
A3		0.20 REF	
b	0.45	0.50	0.55
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	2.25	2.35	2.45
E2	4.00	4.10	4.20
L	0.40	0.50	0.60
e		1.27 BSC	
K		2.10 REF	
K1		0.55 REF	

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
DFN5x6-7	1

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