JW1515H

Offline QR GaN Flyback Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®1515H is a controller for offline flyback with GaN, which features quasi-resonant (QR) operation. QR control improves efficiency by reducing switching loss and also benefits EMI performance with nature frequency variation, and an internal frequency limitation to overcome the inherent disadvantages of QR flyback.

The JW1515H combines PWM and PFM control at different input and load condition for highest average efficiency.

The JW1515H comprises a HV pin for startup to eliminate conventional startup resistor and save standby mode energy consumption. It can comply with the most stringent efficiency regulations. Also, the HV pin is used for X-cap discharge when the AC input is removed, which helps to reduce the X-cap discharge loss and achieve extremely low standby power loss.

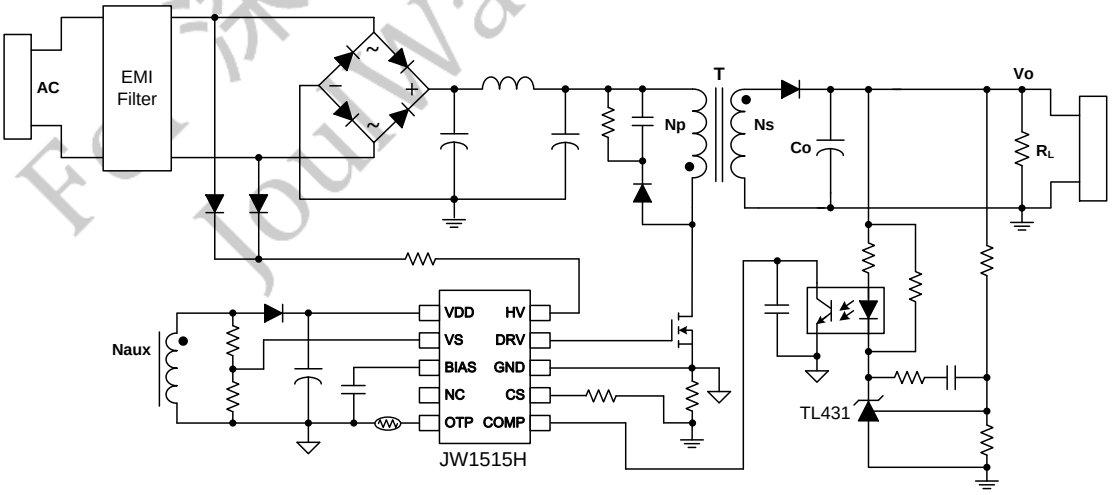
FEATURES

- Built-in High-Voltage Startup (700V)
- 6V Drive Voltage for GaN
- X-Capacitor Discharge Function
- Wider VDD Operation Range (up to 90V)
- QR Operation for High Efficiency
- Maximum 260kHz Switching Frequency
- Optional OCP and OPP Function for Different PD and QC Output Application
- Very Low Standby Power Consumption
- Cycle-by-Cycle Current Limit
- Reliable Fault Protections: VDD OVP, VS OVP and UVP, Brown-In and Brown-Out, CS Open Protection, OCP, OPP, Internal OTP, External OTP
- Frequency Jitter to Ease EMI Compliance
- Available in SSOP-10 Package

APPLICATIONS

- PD and Quick-Charging Chargers
- AC/DC Adapters with Wide Output Range

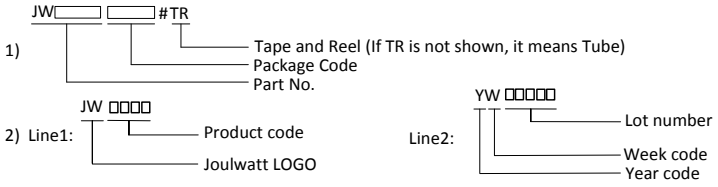
TYPICAL APPLICATION



ORDER INFORMATION

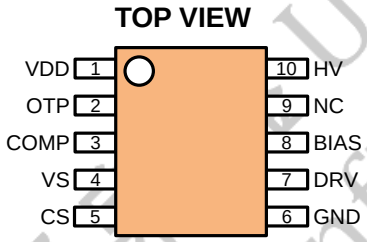
DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW1515HSSOP#TR	SSOP10	JW1515H YW□□□□□	Green

Notes:



3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

HV Voltage 700V
VDD Voltage 100V
OTP, COMP, CS Voltage Range ..... -0.3V to 5V (5V to 5.5V<10us)
DRV, BIAS Voltage Range .....-0.3V to 6.3V (6.3V to 7V<10us)
VS Voltage Range .....-0.3V to 5V (-0.7V to -0.3<10us, 5V to 5.5V<10us)
Junction Temperature[2)3)] 150ºC
Storage Temperature ..... -65ºC to 150ºC
Lead Temperature (Soldering, 10sec.) 260ºC
Continuous Power Dissipation (TA = 25 ºC)[4)] SSOP10.....960mW

RECOMMENDED OPERATING CONDITIONS

VDD Voltage ..... 8 to 88V
Operating Junction Temperature (T_J).....-40ºC to 125ºC

THERMAL PERFORMANCE[5)]

	θ_{JA}	θ_{Jc}
SSOP10	130	...80ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress rating do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW1515H includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA.

5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_A = 25ºC, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
High Voltage Section *(HV Pin)*						
Supply Current from HV Pin	I_{HV}	V_{HV}=120V, VDD=0V		3		mA
Leakage Current of HV Pin	I_{HV_LK}	V_{HV}=500V, VDD=20V		20		uA
Brown-In Threshold	V_{BR_IN}			112		V
Brown-Out Threshold	V_{BR_OUT}			98		V
Brown-Out Blanking Time	t_{BR_OUT}			70		ms
Supply Voltage Section *(VDD Pin)*						
Turn-On Threshold Voltage	V_{DD_ON}	VDD Rising		16.5		V
Turn-Off Threshold Voltage	V_{DD_OFF}	VDD Falling		7.5		V
Reset Threshold Voltage	V_{DD_RST}			4.5		V
Startup Current	I_{DD_ST}	VDD=VDD_ON-0.5 V		80		uA
Operating Supply Current	I_{DD_OP}	VDD=20 V, C_{DRV}=1nF, fs=260kHz		2.5		mA
VDD OVP Voltage	V_{DD_OVP}			90		V
Voltage Sense Section *(VS Pin)*						
Maximum VS Source Current Capability	I_{VS_MAX}			3.5		mA
Output OVP threshold	V_{VS_OVP}			3		V
Output UVP threshold	V_{VS_UVP}			0.25		V
Adaptive Blanking time for VS Sampling	t_{VS_BLK}	COMP=0.5V		0.6		us
		COMP=3.6V		2		us
Output OVP Debounce Cycle Counts	N_{VS_OVP}			3		Cycle
Output UVP Blanking Time	t_{VS_UVP}			120		ms
Auto-Restart Cycles for UVP	N_{UVP_HIC}			4		Cycle
Current Sense Section *(CS Pin)*						
Max CS Offset Current	I_{CS_MAX}	VDD=20V, COMP=3.6V		100		uA
Min CS Offset Current	I_{CS_MIN}	VDD=20V, COMP=0.5V at Burst Mode		25		uA
CS Off Threshold	V_{CS_TH}			20		mV
Leading-Edge Blanking Time	t_{LEB}			150		ns
OCP Enable Threshold	V_{OCP_EN}			0.65		V
OCP Blanking Time	t_{OCP_BLK}			120		ms
OCP Internal Threshold	V_{OCP}			0.2		V

Auto-Restart Cycles for OCP	N_{OCP_HIC}			4		Cycle
Frequency Jittering Section						
Frequency Jittering Amplitude to COMP	ΔF_{JIT}			±7%		
Counting Cycles for Jittering	N_{JIT_CYC}			32		Cycle
Drive Section *(DRV Pin)*						
Gate Output Voltage Low	V_{DRV_L}				0.5	V
Gate Output Clamping Voltage	V_{DRV_CLAMP}	VDD=20V		6		V
Rising Time	t_r			50		ns
Falling Time	t_f			30		ns
Maximum Source Current	I_{SRC}			100		mA
Maximum Sink Current	I_{SINK}			800		mA
Maximum ON Time	T_{ON_MAX}			18		us
Minimum ON Time	T_{ON_MIN}			180		ns
Maximum Switching Cycle	T_{S_MAX}			80		us
Maximum Switching Frequency	f_{max}			260		kHz
Minimum Switching Frequency	f_{min}			25		kHz
Feedback Section *(COMP Pin)*						
Open Pin Voltage	V_{COMP_MAX}	Open Loop		4.0		V
Internal Pull-Up Resistor	R_{COMP_UP}			20		kΩ
COMP to CS offset current Gain	G_{COMP_CS}	COMP>2.8V (@ QR mode)		20		V/mA
		COMP<1V (@ DPWM mode)		16		V/mA
The Threshold Enter PFM Mode	V_{COMP_PFM}			2.8		V
The Threshold Enter Burst Mode	V_{BUR_L}			0.5		V
The Threshold Exit Burst Mode	V_{BUR_H}			0.6		V
OPP Blanking Time	t_{OPP_BLK}			120		ms
OPP Internal Threshold	V_{OPP}			0.8		V
Auto-Restart Cycles for OPP	N_{OPP_HIC}			4		Cycle
Over Load Protection Threshold	V_{OLP}			3.6		V
OLP Blanking Time	t_{OLP_BLK}			120		ms
Auto-Restart Cycles for OLP	N_{OLP_HIC}			4		Cycle
External Over Temperature Protection*(OTP Pin)*						
Over Temperature Protection (OTP) Enter Threshold	V_{OTP_IN}			250		mV
Over Temperature Protection (OTP) Exiting Threshold	V_{OTP_OUT}			500		mV
OTP Pull-Up Current Source	I_{OTP}			25		uA

Internal Over Temperature Protection						
Thermal Shutdown Threshold	T_{OTP}			140		°C
OTP Hysteresis	T_{HYS}			30		ºC

PIN DESCRIPTION

Pin SSOP10	Name	Description
1	VDD	Bias power input to the controller. A hold-up capacitor to GND is required.
2	OTP	External temperature sensing pin. An external NTC (negative temperature coefficient) thermistor to GND is required.
3	COMP	Feedback input pin for flyback QR controller. Connect to an opto-coupler directly.
4	VS	Voltage sensing input pin. Coupled to the auxiliary winding via a resistor divider to monitor the output voltage for OVP and UVP protection. This pin also detects the resonant valley for QR operation.
5	CS	Current sensing input pin. This pin sense the primary switch current for peak current control and OCP. Besides, this pin is used to choose OCP or OPP function at the initial start.
6	GND	The ground of the IC.
7	DRV	Gate output pin.
8	BIAS	Bias power of the driver, an external hold-up capacitor to GND is required
9	NC	
10	HV	High voltage input pin. This pin provides source current to charge VDD. This pin is used for X-cap discharge when the AC input is removed. Besides, this pin also sense input voltage for brown-in and brown-out protection.

BLOCK DIAGRAM TBD

FUNCTIONAL DESCRIPTION

The JW1515H is an offline flyback controller with secondary side feedback, which features multi-mode quasi-resonant (QR) operation. The Quasi- Resonant (QR) with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

The JW1515H has an inherent frequency jittering mechanism to improve the EMI performance under QR operation.

1. Start-Up

1.1. HV Start-Up

When HV is connected to rectified AC input, the internal JFET turns on and a HV current source starts to charge VDD cap. As soon as VDD reaches turn-on threshold V_{DD_ON} (16.5V), the internal startup circuit is disabled. The controller is enabled and the converter starts switching. The VDD turn-off threshold (V_{DD_OFF}) is 7.5V.

1.2 Soft-Start

In the absence of a detected fault, the controller begins to work normally along with soft start. The internal soft-start time is within 4 ms with the feedback signal V_{COMP} rising gradually from the minimum level to the maximum level. Every restart up is followed by a soft start.

2. Normal Operation

After the controller start-up, it enters normal operation. The JW1515H realizes output adjustment based on the feedback signal transmitting to the primary-side controller by an opto-coupler.

The JW1515H is a multi-mode QR controller with secondary-side regulation. According to the feedback signal V_{COMP}, the converter operates in different modes for efficiency optimization. Fig.1 illustrates the frequency and peak current amplitude modulation modes. It can be divided into four operation regions as shown in Fig.1.

Under heavy load condition, the system operates in QR mode, the maximum switching frequency is limited to 260kHz. For medium-load range, the Pulse Frequency Modulation (PFM) is used and primary peak current is nearly fixed to achieve high efficiency. When the load is further reduced, switching frequency is fixed at 25kHz along with primary peak current varying from 50% to 25% of its maximum value. When the system is working under very light load condition, the control mode of IC changes to burst mode. When the voltage of COMP pin drops below V_{BUR_L} (0.5V), the drive stops. The drive will resume when the voltage of COMP pin rises back to V_{BUR_H} (0.6V). Otherwise the gate driver remains at off state to minimize switching loss and reduce standby power consumption. Transitions between modes are automatically accomplished by the controller depending on the feedback signal, V_{COMP}.

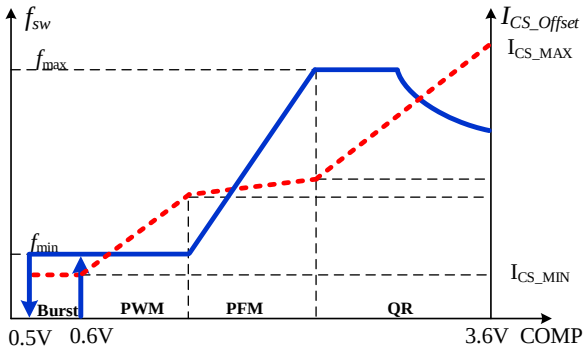


Fig.1 Frequency & Ipk modulation

3. Other Functions and Features

3.1 Frequency Jittering

To achieve good EMI performance, frequency jittering method is integrated in the JW1515H. The frequency jittering is achieved by varying the switching frequency directly. The variation is ±7% around its normal value. The modulation cycle is determined by counting consecutive 32 switching cycles.

3.2 Lead Edge Blanking (LEB)

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) is used between the CS pin and the current comparator input. The current comparator is disabled and can't turn off the external MOSFET during the blanking time. The normal LEB time is around 150ns. Fig.2 shows the leading edge blanking time.

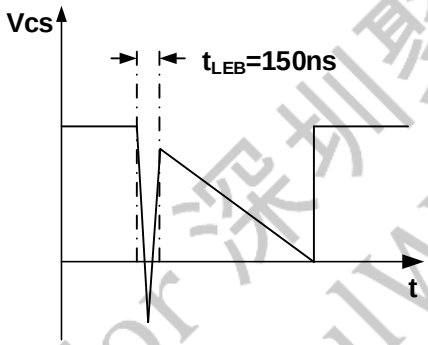


Fig.2 LEB blanking

3.3 CCM Preventing

For the JW1515H, when the primary-side peak current exceeds the value decided by the feedback signal V_{COMP}, the switch turns off. When the controller detects ZCD signal and the switch period exceeds frequency-limit signal, the switch turns on. But the ZCD signal may not be detected during start-up moment because of low output voltage, then the switch will turn on after 80us to make sure the system operates in DCM.

3.4 HV Discharge Function

Safety standards such as UL62368 require that any X-capacitors in EMI filters on the AC side of the bridge rectifier quickly discharge to a safe level when AC is disconnected. The standards require that the voltage across the X-cap decay with a maximum time constant of 2s. Typically, this requirement is achieved by including a resistive discharge element in parallel with the X-cap. However, this resistance causes a continuous power dissipation that impacts the standby power performance.

In order to reduce standby power and eliminate the standing loss associated with the conventional discharge resistors, the JW1515H incorporates X-cap discharge circuit. This circuit periodically monitors the voltage across the X-cap to detect any possibility that AC source disconnection has occurred, and then discharges the voltage across the X-cap using the internal HV current source. The HV discharge function discharges the X-cap to the safety-voltage level in 2s. Fig.3 shows the X-cap discharge timing diagram.

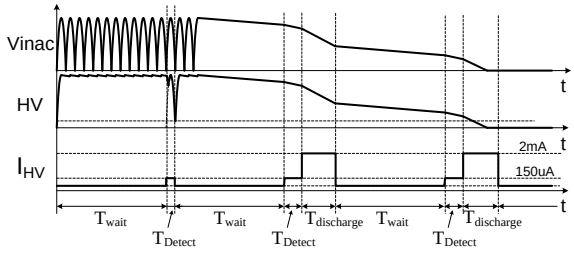


Fig.3 X-cap Discharge

3.5 VS Blanking Time

VS spikes are affected by the amplitudes of Ipk and inductance, so VS blanking time should be set to vary with Ipk. Ensure that the secondary

side conduction time is greater than the VS Blanking Time.

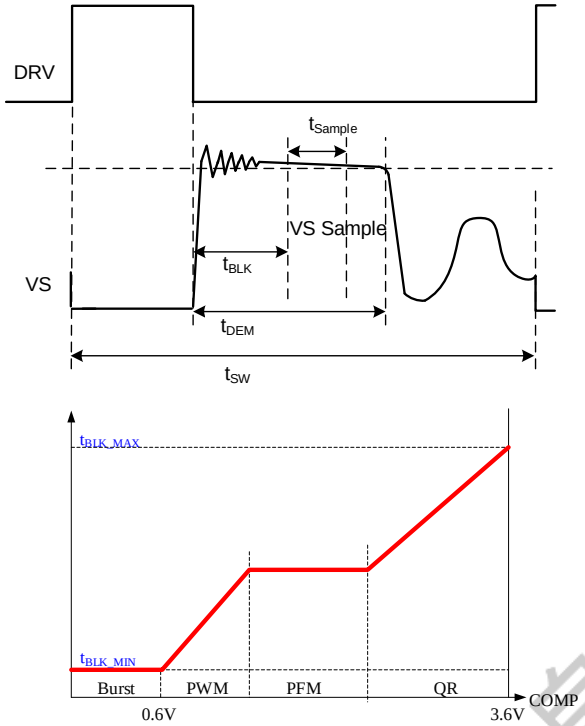


Fig.4 VS blanking time

4. Protection

4.1 CS Pin Open Protection

When CS pin is open, the internal bias current will flow to the parasitic capacitance on the CS pin, increasing the V_{CS}. If V_{CS} is above 2V, a CS pin open fault is triggered.

4.2 Input Brown in / Brown out

The JW1515H senses HV voltage to realize brown in/out function. When HV voltage is higher than V_{BR_IN} (112V typically), a 5mA pull down current will be applied to VDD pin to make VDD hit V_{DD_OFF}. When VDD reaches V_{DD_ON} again, the controller starts switching. And the controller is disabled when HV voltage is lower than V_{BR_OUT} (98V typically) for brown-out blanking time (70ms typically). The blanking time is set long enough to ignore a two cycle drop out. The timer starts counting once HV voltage drops below V_{BR_OUT}.

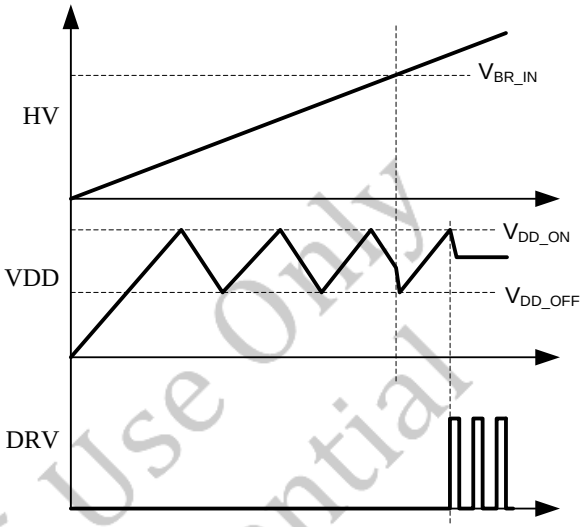


Fig.5 HV Brown-In

4.3 Output OVP (VS OVP)

The output over voltage protection is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 3V for three consecutive switching cycles, an VS_OVP fault is asserted, and then the device shuts down, the UVLO reset and re-start fault cycle begins.

4.4 VS UVP

If the voltage sample on VS pin continues below the under-voltage protection threshold (0.25V) more than 120ms, a VS_UVP fault is asserted. When a VS_UVP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.5 OCP or OPP Selection Circuit

In some PD or QC applications, the maximum output current at different output voltage differs

much. So OCP should be disabled, and the alternative OPP is enabled. The JW1515H senses CS voltage at initial start to determine whether to use OCP or OPP function as Fig.6 shows. At the initial 100us, a 100uA current is applied to CS pin. If CS voltage exceeds a preset enable threshold (typical 0.65V), OPP is enabled and OCP is disabled. Otherwise, OCP is enabled and OPP is disabled.

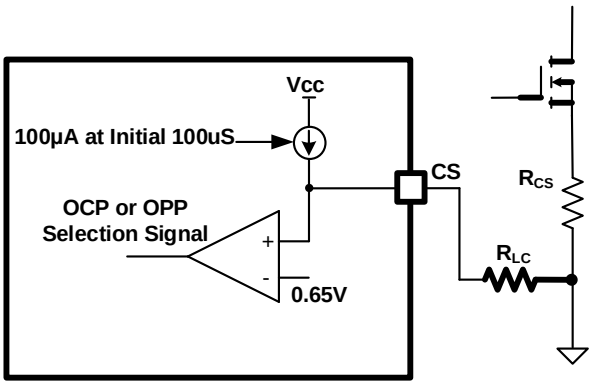


Fig.6 OCP or OPP selection circuit

4.6 OCP

If OCP is enabled, the JW1515H compares estimated output average current and OCP threshold. The output average current is calculated at the primary side. When the primary switch turns off, the peak inductor current (I_{pk}) is sampled and hold for output current calculation.

As shown in Fig.7, it calculates output current based on secondary side current conduction time t_{ons} and primary side current information V_{CS}. If the calculated output current signal, I_{o_est} is higher than the internal OCP threshold V_{OCP} (0.2V typically) for 120ms (OCP blanking time), the JW1515H enters OCP protection.

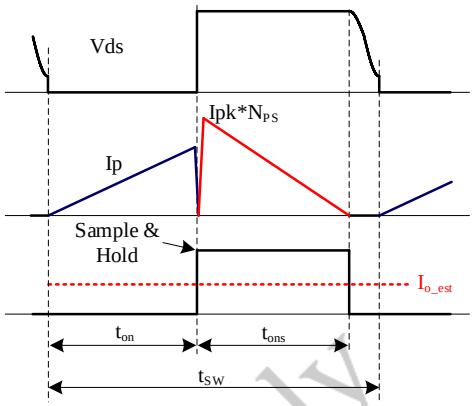


Fig.7 Output current estimation

So the OCP point can be set as:

$$I_o = \frac{V_{ocp} \cdot N_P}{2 \cdot R_{CS} \cdot N_S} \quad (1)$$

wherein, N_P is the turns number of primary winding, N_S is the turns number of secondary winding, R_{CS} is the current sensing resistance.

When an OCP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.7 OPP

If OPP is enabled, the JW1515H compares estimated output power and OPP threshold. The output power is calculated at the primary side based on the estimated output average current in OCP and the output voltage according to the VS voltage. So the output power can be expressed as:

$$P_{out} = I_o \cdot V_o = \frac{V_{CS\_PEAK} \cdot D_S \cdot N_P}{2 \cdot R_{CS} \cdot N_S} \cdot \frac{VS \cdot N_S}{N_{aux}} \cdot \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (2)$$

And the OPP point can be set as:

$$P_{out} = \frac{V_{OPP} \cdot N_P}{2 \cdot R_{CS} \cdot N_{aux}} \cdot \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (3)$$

wherein, N_{aux} is the turns number of auxiliary winding, N_P is the turns number of primary winding.

If the calculated output power signal is higher than the internal OPP threshold V_{OPP} (0.8V typically) for 120ms (OPP blanking timer), the JW1515H enters OPP protection. When an OPP fault is asserted, the device shuts down and the UVLO resets. In order to reduce the power consumption of the circuit, VDD needs to hit V_{DD_OFF} four times, and then the device restarts at the fifth cycle.

4.8 Over Load Protection

If the voltage on COMP pin continues exceeds the over-load protection threshold more than 120ms, an OLP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

4.9 VDD OVP

If the voltage on VDD pin continues exceeds the over-voltage protection threshold (90V typically) more than 100us, a VDD OVP fault is asserted. The device shuts down, then the UVLO reset and re-start fault cycle begins.

4.10 External OTP

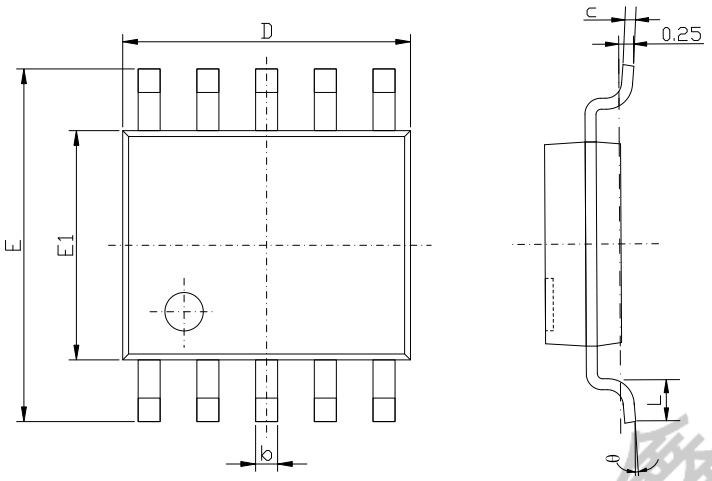
An external NTC resistor (R_{NTC}) is coupled to the OTP pin to program a thermal shutdown temperature. The OTP shutdown threshold (V_{OTP_IN}) of 0.25 V with an internal 25uA current source flowing through R_{NTC} results in a 10kΩ thermistor shutdown threshold. Once the thermistor is lower than 10kΩ, an OTP fault triggered, and the 0.25V threshold is increased to 0.5V. The OTP resistance has to increase above 20kΩ to leave OTP. If user needs to disable this function, a 30kΩ resistor can be used to ensure that the OTP can not be triggered.

4.11 Internal OTP

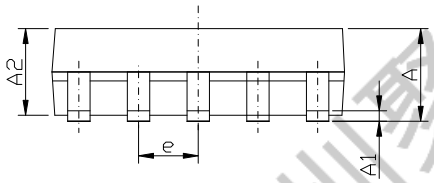
The internal over temperature protection threshold is 140°C. If the junction temperature of the device reaches this threshold, the device shuts down. When the junction temperature falls below 110°C, the device initiates the UVLO reset and re-start fault cycle.

PACKAGE OUTLINE

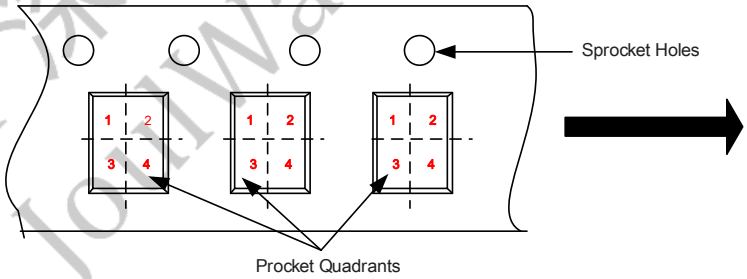
SSOP10 Unit: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.350	1.550	1.750
A1	0.100	0.170	0.250
A2	1.300	—	1.550
b	0.300	—	0.470
c	0.170	0.210	0.250
D	4.700	4.900	5.100
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	1.000 (TYP)		
L	0.400	—	1.270
θ	0°	—	8°



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Package Type	Pin1 Quadrant
SSOP10	1

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